The listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1.-40. (Canceled)

41. (Previously Presented) A method of manufacturing an active matrix type display device comprising the steps of:

forming a gate electrode over an insulating surface of a substrate;

forming a gate insulating film over said gate electrode;

depositing an amorphous semiconductor film comprising silicon on said gate insulating film;

patterning said semiconductor film into an island comprising a channel region;

forming an organic leveling film over said semiconductor film after said patterning thereof to provide a leveled upper surface;

forming an opening in said organic leveling film; and

forming a pixel electrode over said organic leveling film through said opening,

wherein said opening has a tapered configuration so that a diameter thereof is larger at an upper portion than at a lower portion of said opening, and

wherein said upper portion of said opening is rounded from a first point on said leveled upper surface of said leveling film to a second point inside said opening adjacent said upper portion.

42. (Previously Presented) A method according to claim 41 further comprising a step of depositing an n-type semiconductor layer on said amorphous semiconductor film through plasma CVD using a mixture gas containing a silane, phosphine and hydrogen.

43. (Previously Presented) A method according to claim 41 further comprising a step of forming a pair of impurity doped semiconductor layers on said island, wherein one of said impurity doped semiconductor layers is electrically connected with said pixel electrode.

44. (Previously Presented) A method according to claim 41 wherein said gate electrode comprises a doped silicon film and a molybdenum film formed thereon.

45. (Previously Presented) A method according to claim 41 wherein said gate electrode comprises aluminum.

46. (Previously Presented) A method according to claim 41 wherein said gate insulating film comprises silicon oxide.

47. (Previously Presented) A method according to claim 41 wherein said amorphous semiconductor film is deposited through plasma CVD.

48. (Previously Presented) A method according to claim 41 wherein said amorphous semiconductor film is deposited to a thickness of 500 to 5000 Å.

49. (Previously Presented) A method according to claim 41 wherein said organic leveling film directly contacts a portion of said amorphous semiconductor film.

50. (Previously Presented) A method according to claim 41 wherein said pixel electrode extends over said channel region.

51. (Previously Presented) A method of manufacturing an active matrix type display device comprising the steps of:

forming a gate electrode over an insulating surface of a first substrate;

forming a gate insulating film over said gate electrode;

depositing an amorphous semiconductor film comprising silicon on said gate insulating film;

patterning said semiconductor film into an island comprising a channel region;

forming a first organic leveling film over said semiconductor film after said patterning thereof to provide a leveled upper surface;

forming an opening in said organic leveling film;

forming a pixel electrode over said organic leveling film through said opening;

forming a color filter over a second substrate;

forming a second organic leveling film over said color filter;

forming a counter electrode on said second leveling film; and

facing said second substrate to said first substrate so that said counter electrode and said pixel electrode are opposed to each other.

52. (Previously Presented) A method according to claim 51 further comprising a step of depositing an n-type semiconductor layer on said amorphous semiconductor film through plasma CVD using a mixture gas containing a silane, phosphine and hydrogen.

53. (Previously Presented) A method according to claim 51 further comprising a step of forming a pair of impurity doped semiconductor layers on said island, wherein one of said impurity doped semiconductor layers is electrically connected with said pixel electrode.

54. (Previously Presented) A method according to claim 51 wherein said gate electrode comprises a doped silicon film and a molybdenum film formed thereon.

55. (Previously Presented) A method according to claim 51 wherein said gate electrode comprises aluminum.

56. (Previously Presented) A method according to claim 51 wherein said gate insulating film comprises silicon oxide.

57. (Previously Presented) A method according to claim 51 wherein said amorphous semiconductor film is deposited through plasma CVD.

58. (Previously Presented) A method according to claim 51 wherein said amorphous semiconductor film is deposited to a thickness of 500 to 5000 Å.

59. (Previously Presented) A method according to claim 51 wherein said organic leveling film directly contacts a portion of said amorphous semiconductor film.

60. (Previously Presented) A method according to claim 51 wherein said pixel electrode extends over said channel region.

61. (Previously Presented) A method of manufacturing an active matrix type display device comprising the steps of:

forming a gate electrode over an insulating surface of a first substrate;

forming a gate insulating film over said gate electrode;

depositing an amorphous semiconductor film comprising silicon on said gate insulating film;

patterning said semiconductor film into an island comprising a channel region;

forming a first organic leveling film over said semiconductor film after said patterning thereof to provide a leveled upper surface;

forming an opening in said organic leveling film;

forming a pixel electrode over said organic leveling film through said opening;

forming a resin black matrix over a second substrate;

forming a second organic leveling film over said resin black matrix;

forming a counter electrode on said second leveling film; and

facing said second substrate to said first substrate so that said counter electrode and said pixel electrode are opposed to each other.

62. (Previously Presented) A method according to claim 61 further comprising a step of depositing an n-type semiconductor layer on said amorphous semiconductor film through plasma CVD using a mixture gas containing a silane, phosphine and hydrogen.

63. (Previously Presented) A method according to claim 61 further comprising a step of forming a pair of impurity doped semiconductor layers on said island, wherein one of said impurity doped semiconductor layers is electrically connected with said pixel electrode.

64. (Previously Presented) A method according to claim 61 wherein said gate electrode comprises a doped silicon film and a molybdenum film formed thereon.

65. (Previously Presented) A method according to claim 61 wherein said gate electrode comprises aluminum.

66. (Previously Presented) A method according to claim 61 wherein said gate insulating film comprises silicon oxide.

67. (Previously Presented) A method according to claim 61 wherein said amorphous semiconductor film is deposited through plasma CVD.

68. (Previously Presented) A method according to claim 61 wherein said amorphous semiconductor film is deposited to a thickness of 500 to 5000 Å.

69. (Previously Presented) A method according to claim 61 wherein said organic leveling film directly contacts a portion of said amorphous semiconductor film.

70. (Previously Presented) A method according to claim 61 wherein said pixel electrode extends over said channel region.

71. (Previously Presented) A method of manufacturing an active matrix type display device comprising the steps of:

forming a gate electrode over an insulating surface of a first substrate;

forming a gate insulating film over said gate electrode;

depositing an amorphous semiconductor film comprising silicon on said gate insulating film;

patterning said semiconductor film into an island comprising a channel region;

forming a first organic leveling film over said semiconductor film after said patterning thereof to provide a leveled upper surface;

forming an opening in said organic leveling film;

forming a pixel electrode over said organic leveling film through said opening;

forming a color filter over a second substrate;

forming a resin black matrix over said second substrate;

forming a second organic leveling film over said color filter and said resin black matrix;

forming a counter electrode on said second leveling film; and

facing said second substrate to said first substrate so that said counter electrode and said pixel electrode are opposed to each other.

72. (Previously Presented) A method according to claim 71 further comprising a step of depositing an n-type semiconductor layer on said amorphous semiconductor film through plasma CVD using a mixture gas containing a silane, phosphine and hydrogen.

73. (Previously Presented) A method according to claim 71 further comprising a step of forming a pair of impurity doped semiconductor layers on said island, wherein one of said impurity doped semiconductor layers is electrically connected with said pixel electrode.

74. (Previously Presented) A method according to claim 71 wherein said gate electrode comprises a doped silicon film and a molybdenum film formed thereon.

75. (Previously Presented) A method according to claim 71 wherein said gate electrode comprises aluminum.

76. (Previously Presented) A method according to claim 71 wherein said gate insulating film comprises silicon oxide.

77. (Previously Presented) A method according to claim 71 wherein said amorphous semiconductor film is deposited through plasma CVD.

78. (Previously Presented) A method according to claim 71 wherein said amorphous semiconductor film is deposited to a thickness of 500 to 5000 Å.

79. (Previously Presented) A method according to claim 71 wherein said organic leveling film directly contacts a portion of said amorphous semiconductor film.

80. (Previously Presented) A method according to claim 71 wherein said pixel electrode extends over said channel region.

81. (Previously Presented) A method of manufacturing an active matrix type display device comprising the steps of:

forming a gate electrode over an insulating surface of a first substrate;

forming a gate insulating film over said gate electrode;

depositing an amorphous semiconductor film comprising silicon on said gate insulating film;

patterning said semiconductor film into an island comprising a channel region;

forming a first organic leveling film over said semiconductor film after said patterning thereof to provide a leveled upper surface;

forming an opening in said organic leveling film;

forming a pixel electrode over said organic leveling film through said opening;

forming a color filter over a second substrate;

forming a second organic leveling film over said color filter;

forming a counter electrode on said second leveling film; and

facing said second substrate to said first substrate so that said counter electrode and said pixel electrode are opposed to each other,

wherein said opening has a tapered configuration so that a diameter thereof is larger at an upper portion than at a lower portion of said opening, and

wherein said upper portion of said opening is rounded from a first point on said leveled upper surface of said leveling film to a second point inside said opening adjacent said upper portion.

82. (Previously Presented) A method according to claim 81 further comprising a step of depositing an n-type semiconductor layer on said amorphous semiconductor film through plasma CVD using a mixture gas containing a silane, phosphine and hydrogen.

83. (Previously Presented) A method according to claim 81 further comprising a step of forming a pair of impurity doped semiconductor layers on said island, wherein one of said impurity doped semiconductor layers is electrically connected with said pixel electrode.

84. (Previously Presented) A method according to claim 81 wherein said gate electrode comprises a doped silicon film and a molybdenum film formed thereon.

85. (Previously Presented) A method according to claim 81 wherein said gate electrode comprises aluminum.

86. (Previously Presented) A method according to claim 81 wherein said gate insulating film comprises silicon oxide.

87. (Previously Presented) A method according to claim 81 wherein said amorphous semiconductor film is deposited through plasma CVD.

88. (Previously Presented) A method according to claim 81 wherein said amorphous semiconductor film is deposited to a thickness of 500 to 5000 Å.

89. (Previously Presented) A method according to claim 81 wherein said organic leveling film directly contacts a portion of said amorphous semiconductor film.

90. (Previously Presented) A method according to claim 81 wherein said pixel electrode extends over said channel region.

91. (Previously Presented) A method of manufacturing an active matrix type display device comprising the steps of:

forming a gate electrode over an insulating surface of a first substrate;

forming a gate insulating film over said gate electrode;

depositing an amorphous semiconductor film comprising silicon on said gate insulating film;

patterning said semiconductor film into an island comprising a channel region;

forming a first organic leveling film over said semiconductor film after said patterning thereof to provide a leveled upper surface;

forming an opening in said organic leveling film;

forming a pixel electrode over said organic leveling film through said opening;

forming a resin black matrix over a second substrate;

forming a second organic leveling film over said resin black matrix;

forming a counter electrode on said second leveling film; and

facing said second substrate to said first substrate so that said counter electrode and said pixel electrode are opposed to each other,

wherein said opening has a tapered configuration so that a diameter thereof is larger at an upper portion than at a lower portion of said opening, and

wherein said upper portion of said opening is rounded from a first point on said leveled upper surface of said leveling film to a second point inside said opening adjacent said upper portion.

92. (Previously Presented) A method according to claim 91 further comprising a step of depositing an n-type semiconductor layer on said amorphous semiconductor film through plasma CVD using a mixture gas containing a silane, phosphine and hydrogen.

93. (Previously Presented) A method according to claim 91 further comprising a step of forming a pair of impurity doped semiconductor layers on said island, wherein

one of said impurity doped semiconductor layers is electrically connected with said pixel electrode.

94. (Previously Presented) A method according to claim 91 wherein said gate electrode comprises a doped silicon film and a molybdenum film formed thereon.

95. (Previously Presented) A method according to claim 91 wherein said gate electrode comprises aluminum.

96. (Previously Presented) A method according to claim 91 wherein said gate insulating film comprises silicon oxide.

97. (Previously Presented) A method according to claim 91 wherein said amorphous semiconductor film is deposited through plasma CVD.

98. (Previously Presented) A method according to claim 91 wherein said amorphous semiconductor film is deposited to a thickness of 500 to 5000 Å.

99. (Previously Presented) A method according to claim 91 wherein said organic leveling film directly contacts a portion of said amorphous semiconductor film.

100. (Previously Presented) A method according to claim 91 wherein said pixel electrode extends over said channel region.

101. (Previously Presented) A method of manufacturing an active matrix type display device comprising the steps of:

forming a gate electrode over an insulating surface of a first substrate;

forming a gate insulating film over said gate electrode;

depositing an amorphous semiconductor film comprising silicon on said gate insulating film;

patterning said semiconductor film into an island comprising a channel region;

forming a first organic leveling film over said semiconductor film after said patterning thereof to provide a leveled upper surface;

forming an opening in said organic leveling film;

forming a pixel electrode over said organic leveling film through said opening;

forming a color filter over a second substrate;

forming a resin black matrix over said second substrate;

forming a second organic leveling film over said color filter and said resin black matrix;

forming a counter electrode on said second leveling film; and

facing said second substrate to said first substrate so that said counter electrode and said pixel electrode are opposed to each other,

wherein said opening has a tapered configuration so that a diameter thereof is larger at an upper portion than at a lower portion of said opening, and

wherein said upper portion of said opening is rounded from a first point on said leveled upper surface of said leveling film to a second point inside said opening adjacent said upper portion.

102. (Previously Presented) A method according to claim 101 further comprising a step of depositing an n-type semiconductor layer on said amorphous semiconductor film through plasma CVD using a mixture gas containing a silane, phosphine and hydrogen.

103. (Previously Presented) A method according to claim 101 further comprising a step of forming a pair of impurity doped semiconductor layers on said

island, wherein one of said impurity doped semiconductor layers is electrically connected with said pixel electrode.

104. (Previously Presented) A method according to claim 101 wherein said gate electrode comprises a doped silicon film and a molybdenum film formed thereon.

105. (Previously Presented) A method according to claim 101 wherein said gate electrode comprises aluminum.

106. (Previously Presented) A method according to claim 101 wherein said gate insulating film comprises silicon oxide.

107. (Previously Presented) A method according to claim 101 wherein said amorphous semiconductor film is deposited through plasma CVD.

108. (Previously Presented) A method according to claim 101 wherein said amorphous semiconductor film is deposited to a thickness of 500 to 5000 Å.

109. (Previously Presented) A method according to claim 101 wherein said organic leveling film directly contacts a portion of said amorphous semiconductor film.

110. (Previously Presented) A method according to claim 101 wherein said pixel electrode extends over said channel region.

111. (New) A method of manufacturing an electro-optical device comprising the steps of:

forming a thin film transistor over a first substrate;

forming a surface flattening film over said thin film transistor;

forming a pixel electrode over said surface flattening film;

forming a color filter over a second substrate;

forming a leveling film over the color filter;

forming a common electrode over the leveling film;

interposing a nematic liquid crystal composition between said first substrate and said second substrate; and

sealing a periphery of the first and second substrates with an adhesive after interposing said nematic liquid crystal therebetween.

112. (New) A method of manufacturing an electro-optical device comprising the steps of:

forming a thin film transistor over a first substrate;

forming a surface flattening film over said thin film transistor;

forming a pixel electrode over said surface flattening film;

forming a color filter over a second substrate;

forming a leveling film over the color filter;

forming a common electrode over the leveling film;

means for orienting liquid crystal molecules provided over said second substrate;

interposing a nematic liquid crystal composition between said first substrate and said second substrate; and

sealing a periphery of the first and second substrates with an adhesive after interposing said nematic liquid crystal therebetween.

113. (New) A method of manufacturing an electro-optical device comprising the steps of:

forming a thin film transistor over a first substrate;

forming a surface flattening film over said thin film transistor;

forming a pixel electrode over said surface flattening film;

forming a color filter over a second substrate;

forming a leveling film over the color filter;

forming a common electrode over the leveling film;

means for orienting liquid crystal molecules provided over said second substrate;

interposing a nematic liquid crystal composition between said first substrate and said second substrate;

sealing a periphery of the first and second substrates with an adhesive after interposing said nematic liquid crystal therebetween;

connecting a PCB comprising a driver IC to a lead over said first substrate; and

affixing a polarizing plate to an outside of the first substrate.

114. (New) The method according to any one of claims 111, 112 and 113 wherein said adhesive is an epoxy adhesive.

115. (New) The method according to any one of claims 111, 112 and 113 wherein said pixel electrode comprises a transparent conductive film.

116. (New) The method according to any one of claims 111, 112 and 113 wherein said common electrode comprises a transparent conductive film.

117. (New) The method according to any one of claims 111, 112 and 113 wherein said surface flattening film comprises an organic resin.

118. (New) The method according to any one of claims 111, 112 and 113 wherein said first and second substrates are glass substrates.

119. (New) The method according to any one of claims 111, 112 and 113 wherein said nematic liquid crystal is formed by using a die-cast method.

120. (New) A method of manufacturing a television set having a liquid crystal panel comprising the steps of:

forming a thin film transistor over a first substrate;

forming a surface flattening film over said thin film transistor;

forming a pixel electrode over said surface flattening film;

forming a color filter over a second substrate;

forming a leveling film over the color filter;

forming a common electrode over the leveling film;

interposing a nematic liquid crystal composition between said first substrate and said second substrate; and

sealing a periphery of the first and second substrates with an adhesive after interposing said nematic liquid crystal therebetween, thus manufacturing a liquid crystal panel;

providing said liquid crystal panel with a back light device; and

connecting said liquid crystal panel to a tuner for receiving TV electric waves.

121. (New) A method of manufacturing an electro-optical device comprising the steps of:

forming a thin film transistor over a first substrate;

forming a surface flattening film over said thin film transistor;

forming a pixel electrode over said surface flattening film;

forming a color filter over a second substrate;

forming a leveling film over the color filter;

forming a common electrode over the leveling film;

means for orienting liquid crystal molecules provided over said second substrate;

interposing a nematic liquid crystal composition between said first substrate and said second substrate; and

sealing a periphery of the first and second substrates with an adhesive after interposing said nematic liquid crystal therebetween, thus manufacturing a liquid crystal panel;

providing said liquid crystal panel with a back light device; and

connecting said liquid crystal panel to a tuner for receiving TV electric waves.

122. (New) A method of manufacturing an electro-optical device comprising the steps of:

forming a thin film transistor over a first substrate;

forming a surface flattening film over said thin film transistor;

forming a pixel electrode over said surface flattening film;

forming a color filter over a second substrate;

forming a leveling film over the color filter;

forming a common electrode over the leveling film;

means for orienting liquid crystal molecules provided over said second substrate;

interposing a nematic liquid crystal composition between said first substrate and said second substrate;

sealing a periphery of the first and second substrates with an adhesive after interposing said nematic liquid crystal therebetween;

connecting a PCB comprising a driver IC to a lead over said first substrate; and

affixing a polarizing plate to an outside of the first substrate, thus manufacturing a liquid crystal panel;

providing said liquid crystal panel with a back light device; and

connecting said liquid crystal panel to a tuner for receiving TV electric waves.

123. (New) The method according to any one of claims 120, 121, and 122 wherein said adhesive is an epoxy adhesive.

124. (New) The method according to any one of claims 120, 121, and 122 wherein said pixel electrode comprises a transparent conductive film.

125. (New) The method according to any one of claims 120, 121, and 122 wherein said common electrode comprises a transparent conductive film.

126. (New) The method according to any one of claims 120, 121, and 122 wherein said surface flattening film comprises an organic resin.

127. (New) The method according to any one of claims 120, 121, and 122 wherein said first and second substrates are glass substrates.

128. (New) The method according to any one of claims 120, 121, and 122 wherein said nematic liquid crystal is formed by using a die-cast method.